Exploiting the effect of noise on nonlinear systems to obtain reconfigurable logic gates

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Abstract: We introduce a scheme to obtain logic gates, which form the basis of universal general-purpose computing devices, using the phenomena of stochastic resonance. The idea is to exploit the effect of noise on nonlinear systems in order to extract different desired responses from it. We demonstrate the principle explicitly by implementing the fundamental NOR and NAND gates, which are the necessary and sufficient components of modern computer architecture. We also demonstrate that one can efficiently switch logic behaviour by simply varying noise levels. Thus using the interplay between nonlinearity and noise one can obtain reconfigurable abilities, allowing the system to flexibly morph its logic operations.

In recent years, the wide-ranging temporal patterns of a nonlinear system have been harnessed to do computational tasks, the so-called "chaos computing" paradigm [1]. The aim is to use a single dynamical unit to emulate different logic gates and perform different arithmetic tasks, and further have the ability to switch easily between the different operational roles. Such a computing unit may then allow a more dynamic computer architecture and serve as ingredients of a general-purpose reconfigurable device more versatile and flexible than statically wired hardware [2]. This new approach to computing has great potential to accelerate a wide variety of applications and seeks to combine the general utility of conventional Central Processing Units (CPUs) with the optimization and speed of Application Specific Integrated Circuits (ASICs).

Here we will present a new direction in exploiting nonlinear physical phenomena for computations: namely we will introduce a scheme for *noise-assisted* computation which uses the phenomena of *stochastic resonance* to obtain different logic responses. We will demonstrate the general principle of the scheme by explicit implementation of the *fundamental* NOR and NAND gates, which form the basis of universal computing machines [3]. Further we will show how one can dynamically switch between these logic responses using varying noise levels.

Now stochastic resonance (SR) has received much attention over the past few decades [4]. Generally be considered as the phenomena whereby weak input information (such as a feeble signal) can be amplified and optimized under noise that is

Logic gate	Input Set (I_1,I_2)	Output
NOR	(0,0)	1
	(0,1)/(1,0)	0
	(1,1)	0
NAND	(0,0)	1
	(0,1)/(1,0)	1
	(1,1)	0

Table 1: Input sets and the output of the fundamental 2-inputs NOR and NAND operations.

inherent in the system or that adds to the input. We exploit this simple, robust and rather well understood principle, to do a hitherto unexplored task, namely we use it to construct logic gates [1].

Scheme for obtaining logic gates

First we outline the general scheme for implementing the fundamental NOR and NAND logic gates. Table 1 displays the truth table of 2-input NOR and NAND gates, with the last column giving the output O corresponding to the two inputs I_1 and I_2. Note that the four distinct possible input sets $(0,0)$, $(0,1)$, $(1,0)$ and $(1,1)$ reduce to three conditions as $(0,1)$ and $(1,0)$ are symmetric.

A logic cell here is comprised of a nonlinear system, given by:

$$\dot{x} = F(x) + I + C + D\eta(t) \tag{1}$$

where $F(x)$ is a nonlinear function giving rise to a double-well potential (with the wells centered around x_+ and x_-). I is a *low amplitude* input signal, C is a constant bias and $\eta(t)$ is an additive zero-mean Gaussian noise with variance 1. The parameter D gives the noise strength. Such a system typically is capable of displaying SR, with the state switching between the two wells x_+ and x_- (see Fig. 2 for an example).

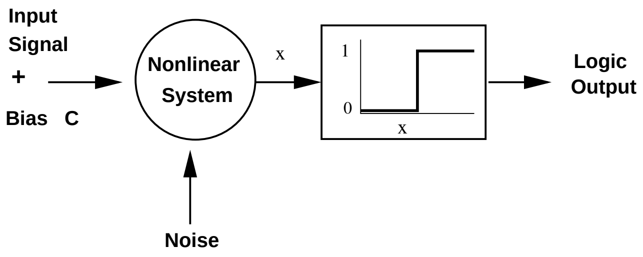

Figure 1: Schematic diagram of a logic cell comprised of a nonlinear system forced by an input signal, plus noise and a constant bias, either of which can act as a logic response controller.

Setting Inputs : The inputs determine the low amplitude signal I in the above system (see schematic in Fig. 1). For instance for 2-input gates : $I = I_1 + I_2$, where I_1 and I_2 encode the two logic inputs.

Obtaining Output : The logic output will be given as follows:

(i) If $x > 0$, Logic Output is 0

(ii) If $x < 0$, Logic Output is 1

Logic Gate Control : In our scheme one can manipulate the logic response by using either of the following:

(i) the bias parameter C

(ii) the noise level D

(iii) the nonlinearity

Namely, by changing either the noise amplitude, or the bias, or the nonlinearity, one can switch between logic functions.

Now we explicitly demonstrate the general idea above with a simple system that shows stochastic resonance. The system we propose to use as the basic logic cell has the advantage that the *only nonlinearity* in the system is implemented by a simple thresholding mechanism.

Specifically, under additive noise of amplitude D, it is given by:

$$\dot{x} = -\alpha x + \beta\, g(x) + I + C + D\, \eta(t) \tag{2}$$

The nonlinear function $g(x)$ is a *piecewise linear function* that is particularly easy to implement:

$$\begin{aligned} g(x) &= x \quad \text{when} \quad x_l^* \leq x \leq x_u^* \\ g(x) &= x_l^* \quad \text{when} \quad x < x_l^* \\ g(x) &= x_u^* \quad \text{when} \quad x > x_u^* \end{aligned} \tag{3}$$

where x_u^* and x_l^* are the upper and lower thresholds respectively (see Fig. 2). An advantage of this piecewise-linear function is that it can be realized by an extremely simple experimental circuit. The response of this system under varying noise amplitudes, both additive and multiplicative, display enhanced response in a window of D (see Fig. 3 for an illustrative example of the response of the system to an aperiodic stream of pulses).

The stochastic resonance in this system can be clearly understood if one inspects the effective potential generated by the thresholding (see Fig. 2). The effective potential is a *double well*, a scenario where SR is very well elucidated [4]. The position of the wells are given by $x_- = (\beta x_l^* + C)/\alpha$ and $x_+ = (\beta x_u^* + C)/\alpha$. So the heights and asymmetry of the wells can be manipulated very easily by simply setting different thresholds x_l^* and x_u^*, or by varying bias C, as is evident in Fig. 2. Characteristic signatures of SR are observed in this system, e.g. in the dependence of the SNR on noise level D.

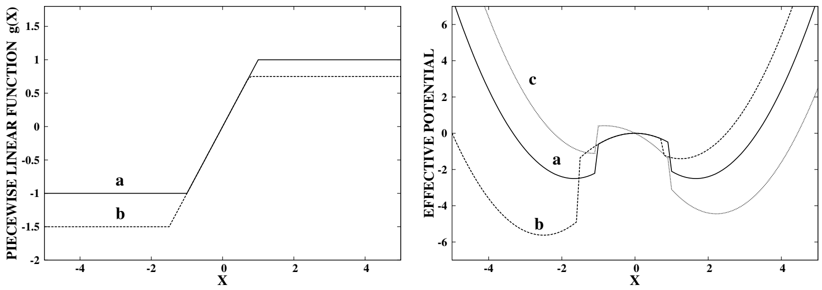

Figure 2: For the system in Eqn. 2, (left) the piecewise linear function $g(x)$ and (right) the effective potential it gives rise to, with thresholds (a) $x_l^* = -1, x_u^* = 1$ (solid line) and (b) $x_l^* = -1.5, x_u^* = 0.75$ (dashed line) and (c) $x_l^* = -1, x_u^* = 1$ with bias $C = 1$ (dotted line). Equal upper and lower thresholds (i.e. $x_l^* = x_u^*$) give rise to symmetric wells, while unequal thresholds produce asymmetric wells. Further nonzero bias C can give rise to asymmetry as in case (c) in (ii)

With this system now one can obtain different logic gates by implementing the general logic control schemes outlined earlier. Specifically, in Eqn. 2, we take $\alpha = 1.8, \beta = 3.0$, and (i) $I_1 \ / \ I_2 = -0.4$ when logic input is 0 and (ii) $I_1 \ / \ I_2 = 0.4$ when logic input is 1.

I. *Obtaining the desired logic responses by manipulating the constant bias :*

Fig. 4 shows the dynamics of the system under different noise levels D, and with different bias C. The remarkable thing here is that noise helps to select the desired responses from this nonlinear system. For very small and very large noise the system does not yield the requisite response. But in an optimal window of noise, it yields the correct logic response. As the value of the bias C is switched, the response of the system switches from NOR to NAND logic, or vice a versa. Representative values of C which yield the NOR and NAND gates (with thresholds $x_l^* = -1$ and $x_u^* = 1.8$) are 0 and -0.8 respectively, under noise level $D \sim 2$.

II. *Obtaining the desired logic responses by manipulating noise levels:*

Alternately, one can keep the bias C constant and change the noise level D to switch between gates. Fig. 5 displays an illustrative example demonstating how noise levels can act as logic response controllers in this system. Representative noise levels D yielding the NOR and NAND logic responses (with bias $C = 0$, and thresholds $x_l^* = -1$ and $x_u^* = 1.8$) are 1.8 and 2.6 respectively.

III. *Obtaining the desired logic responses by manipulating the thresholds:*

Lastly, one can also use the thresholds defining nonlinearity $g(x)$ in eqn. 2 as logic

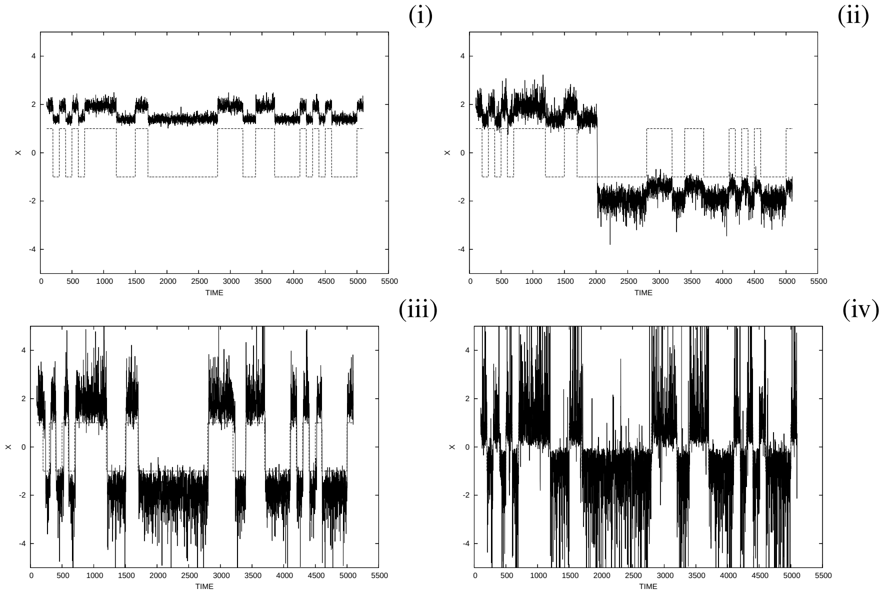

Figure 3: Time series of x arising from the system given by Eqn. 3, where $C = 0$ and the piecewise linear function $g(x)$ has thresholds $x_l^* = -1$, $x_u^* = 1$, for multiplicative noise levels D equal to (i) 1 (ii) 1.75 (iii) 2.5 (iv) 4. The input I is an *aperiodic* train of square pulses (i.e. I switches from 1 to -1 at random intervals), and is shown as a dashed line. It is evident that for intermediate noise the system has the largest response to the external impulse.

controllers. Changing a threshold, as in evident from Fig. 2, changes the position and depth of the wells in the effective potential. By switching a threshold one can switch between logic responses as well. This is demonstrated in Fig. 6, with representative values of the upper threshold $x_u^* \sim 1$ giving the NOR and $x_u^* \sim 0.5$ giving the NAND response (with $D = 1.5$ $x_l^* = -1$ and $C = 0$).

Proof-of-principle experiments have also been carried out with analog simulation circuits shown in Fig. 7, and the results are in complete agreement with the numerics.

Further, while in this explicit example we have implemented 2-input logic gates, the scheme can be easily extended to *multiple input logic gates*. In particular, we have demonstrated 3-input logic gates with the system, with the input signal being $I = I_1 + I_2 + I_3$.

We have also checked the *generality of the scheme* over a range of thresholds and noise levels. Moreover we have also implemented the fundamental NOR gate by exploiting SR in the bistable Schmitt Trigger.

Clearly the operational speeds attainable by such a dynamic logic cell will be determined by the natural timescales of the dynamical system. So it is evident that the scheme could potentially work at considerable speeds if one can implement it on fast dynamical systems, such as electronic circuits operating in the GHz regime and semi-

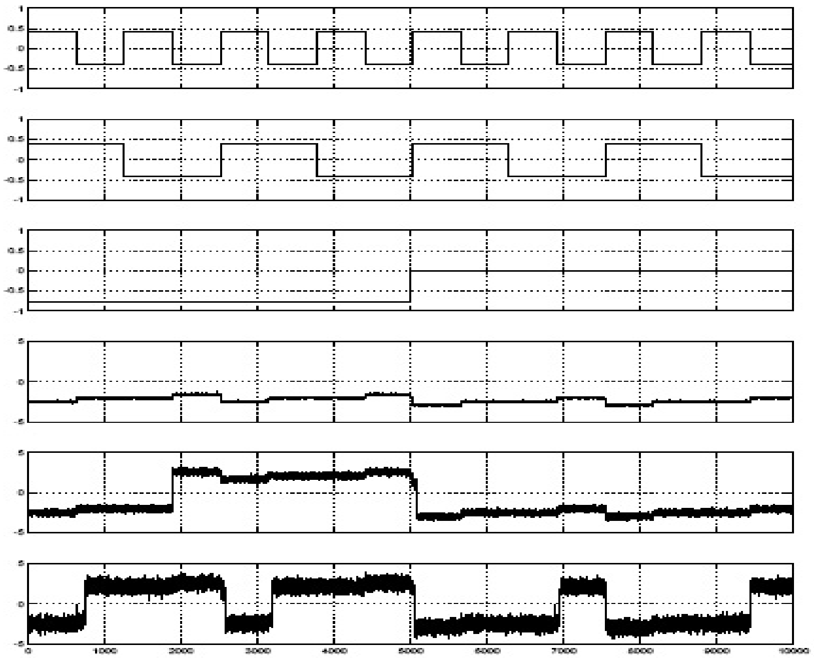

Figure 4: Timing Pulses from top to bottom: panel 1 and 2 show a stream of input signals I_1 and I_2, with $I_1/I_2 = -0.4$ when logic input is 0 and (ii) $I_1/I_2 = 0.4$ when logic input is 1 ; panel 3 shows the bias signal C ($C = -0.8$ for NAND and $C = 0$ for NOR); panels 4-6 show $-x$ of the system given by Eqn. 2, with $x_u^* = 1.8, x_l^* = -1.0$, under noise levels: (i) 0.2 (ii) 1.0 (iii) 2.5. When the noise level is optimum (panel 6) one obtains the desired logic output (NAND response for [0:5000] sec, and NOR response for (5000:10000] sec), while for small noise one does not obtain the necessary response.

conductor lasers yielding chaotic sub nanosecond/picosecond pulses.

In summary, we have used a new physical principle for an ubiquitous application. Namely, we have proposed the use of the dynamical phenomena of stochastic resonce in nonlinear systems for the design of key logic-gate structures. We have demonstrated the idea explicitly on a piecewise-linear system, that has a particularly simple experimental realization. Specifically we have shown the direct and flexible implementation of the fundamental logic gates NOR and NAND, from which any universal computing device can be constructed. Further, we have demonstrated the *switching of logic functions*, with the noise acting as a "logic response controller". Thus the effect of noise on a nonlinear system has been exploited to obtain the basic ingredients of general purpose hardware that has potential for reconfigurability.

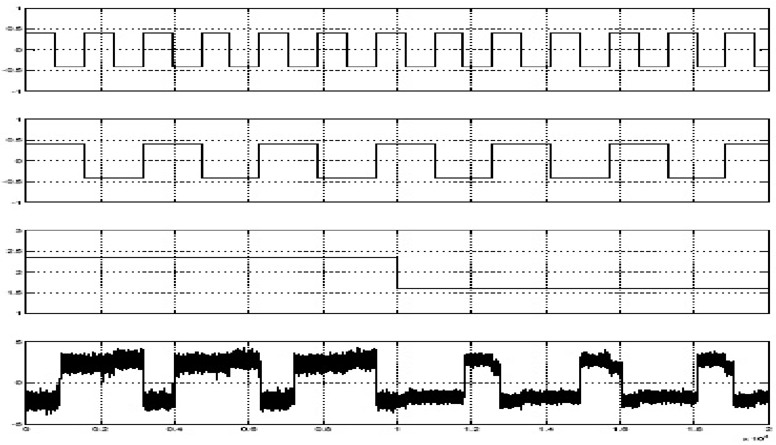

Figure 5: Timing Pulses from top to bottom: panel 1 and 2 show a stream of input signals I_1 and I_2, with $I_1/I_2 = -0.4$ when logic input is 0 and (ii) $I_1/I_2 = 0.4$ when logic input is 1; panel 3 shows the noise amplitude D; panel 4 shows $-x$ of the system given by Eqn. 2, with $x_u^* = 1.8, x_l^* = -1.0, C = 0$. The state of the system yields the desired dynamic logic output: [0-10000] sec is the NAND response, (10000-20000] sec is the NOR response. Clearly noise can control the logic behaviour of the system.

References

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[2] See Taubes, G., *Science* **277** (1997) 1935, for a general discussion of the advantages of reconfigurable computer architectures in the context of Field Programmable Gate Arrays (FPGAs). For introduction to reconfigurable dynamics-based hardware, see : T. Munakata *et al*, IEEE *Trans. Circ. and Systems* **49** (2002) 1629; K. Murali and S. Sinha, *Phys. Rev. E* **75** (2007) R025201.

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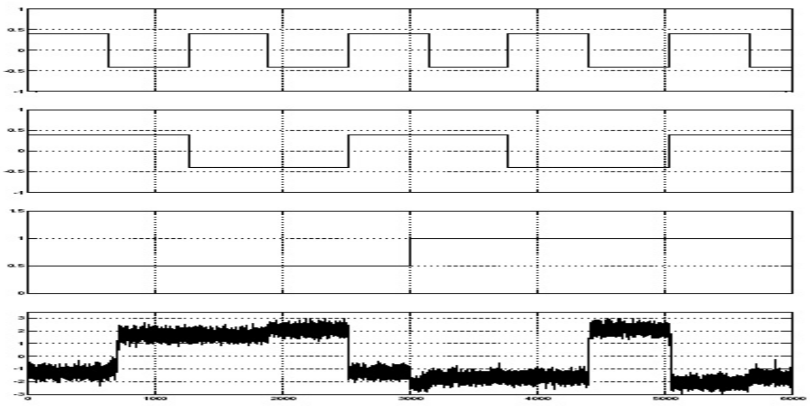

Figure 6: Timing Pulses from top to bottom: panel 1 and 2 show a stream of input signals I_1 and I_2, with $I_1/I_2 = -0.4$ when logic input is 0 and (ii) $I_1/I_2 = 0.4$ when logic input is 1; panel 3 shows the upper threshold x_u^* ($x_l^* = -1, C = 0, D = 1.5$); panel 4 shows $-x$ giving a dynamic logic response: [0-3000] sec is the NAND response, (3000-6000] sec is the NOR response.

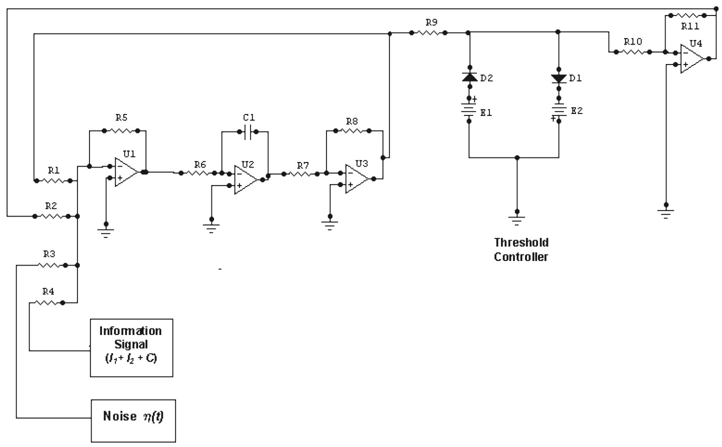

Figure 7: Analog simulation circuit of Eqn. 2