Qubit Arrangement Problems for Topological Quantum Computation

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Background.
To realize a quantum computation, we need to have *fault-tolerant* quantum gates, i.e., quantum gates with a very low operational error rate. We use quantum error correction codes for that purpose in the conventional quantum circuit model.

Topological quantum computation [1] is another possible way to have fault-tolerant quantum gates. Recently, this model of quantum computation has been considered to be much more promising than conventional model of quantum circuits in terms of error corrections. The way of encoding logical qubits in topological quantum computation is very different from the conventional quantum circuit model, and thus the logical primitive operations are also very different. The primitive operation called a *braiding operation* can be seen as drawing a line between logical qubits with some special rules. We need to consider such special rules when we design a quantum circuit. Therefore, it should be difficult to utilize the conventional quantum circuit design naively, and thus it is desirable to have a dedicated quantum circuit optimization method in logic level with considering special rules of braiding operations.

Our Contribution.
In our work, we formulate a quantum circuit optimization problem especially for the topological quantum computation. First we observe that our design strategy should be different from the conventional quantum circuit design as follows. To understand the difference, let us see the circuit in Fig. 1. In the conventional quantum circuit model, we often assume that multiple CNOT gates can be performed at the same time if their interacting qubits are different, and the *depth* of a circuit is calculated based on this assumption. For example, we can perform g_1 and g_2 in the circuit in Fig. 1 at the same time. The important observation here is that such a relation of two gates does not change even if we change the qubit order (qubit layout). Thus, in the conventional quantum circuit design, we do not need to consider the qubit order.

Contrary to the above, in topological quantum computation, we can assume any two gates can be performed parallelly only if their gate symbols on the circuit diagram are not overlapped in the horizontal direction. (The rigorous discussion can be found in the attachment.) For example, we cannot perform g_1 and g_2 in the circuit in Fig. 1 at the same time unlike the conventional circuit model.

Therefore, the qubit orders (i.e., qubit layout) may be really important for the computation time for topological quantum computation. Our problem is intuitively to find a good qubit order for a given circuit as shown in Fig. 1. By our proposed method, we can optimize the circuit in Fig. 1 to the one in Fig. 2. Here, the two circuits are logically equivalent but with different initial

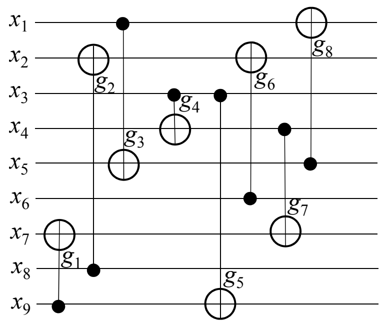

Figure 1: An Initial Circuit: 8 Steps.

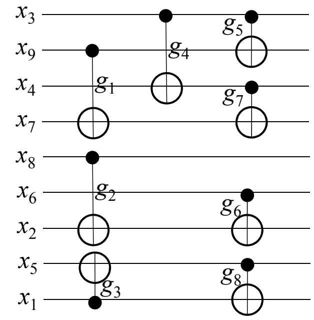

Figure 2: The Optimized One-Dimensional Qubit Layout by Our Method: 3 Steps.

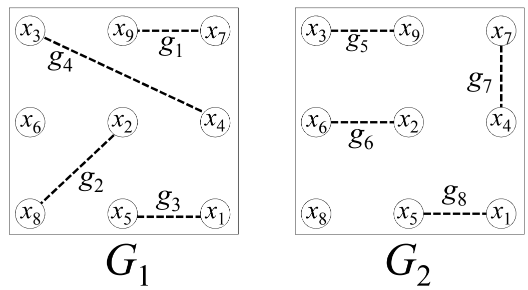

Figure 3: The Optimized Two-Dimensional Qubit Layout by Our Method: 2 Steps.

qubit orders. The number of the logical time steps in the circuit in Fig. 1 is 8, which is optimized by our method to be 3 as shown in Fig. 2.

Moreover we consider two-dimensional qubit layout. In one-dimensional qubit layout, it can be shown that one single qubit order does not allow us to perform the above circuit with two time steps. For example, at the one-dimensional qubit layout of the qubit order as shown in Fig. 2, the three gates, g_4, g_1 and g_5 (or g_7), are overlapped with each other; we need at least three time steps. In contrast, if we layout the qubits two-dimensionally as shown in Fig. 2, we can perform the circuit with only two logical time steps. This is because the two-dimensional qubit layout allows us to perform g_1, g_2, g_3 and g_4 at the same time as shown on the left-hand side of Fig. 3. Our proposed method can find such a good two-dimensional qubit layouts efficiently. As far as we know, our method is the first systematic synthesis method for topological quantum circuits by considering two-dimensional qubit layouts. Both of our optimization methods for one-dimensional and two-dimensional layouts utilize clique finding efficiently. The detail is discussed in the attachment.

References

[1] Austin G. Fowler, Ashley M. Stephens, and Peter Groszkowski. High threshold universal quantum computation on the surface code. *PHYS.REV.A*, 80:052312, 2009.