

A NEW REVERSIBLE SMG GATE AND ITS APPLICATION FOR DESIGNING REVERSIBLE TWO'S COMPLEMENT ADDER/SUBTRACTOR

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ABSTRACT

Reversible computation plays an important role in the synthesis of circuits having application in quantum computing, low power CMOS design, bioinformatics and nanotechnology based systems. Conventional logical circuits are not reversible. A reversible circuit maps each input vector, into a unique output vector and vice versa. A new 4×4 reversible full adder gate called as SMG gate is suggested in this paper. Three approaches to design reversible adder/subtractor are also proposed for the first time in the literature. The first approach is based on the Toffoli and Feynman gates, second approach is based on the Peres gate and the third approach is based on the new SMG gate. The proposed reversible adder/subtractor circuits are evaluated in terms of number of reversible gates, number of garbage outputs, number of constant inputs and quantum cost.

Keywords: Reversible gates, Quantum Computer, Quantum cost, Quantum gates, two's complement adder/subtractor

INTRODUCTION

Many scientists say that “single atom transistor is the end of Moore's law” [1], which states that “within a period of 18 months the number of transistors in an IC doubles all along with its efficiency”. He also predicted that the addition of extra number of transistors will not be possible in next few years and even if so, it may cause power consumption problems. Also, according to Landauer's principle, loss of 1 bit of information dissipates at least $kT \ln 2$ joule of energy, where $k=1.3806505 \times 10^{-23} \text{ m}^2 \text{ kgs}^{-2} \text{ K}^{-1}$ (Joule/Kelvin) is the Boltzman constant and T is the operating temperature [2]. Bennett showed that $kT \ln 2$ energy dissipation would not occur if a computation is carried out in a reversible way [3]. A design which does not result in information loss is reversible. Classical gates AND, XOR, NAND, etc are essentially irreversible or non-invertible. For example, knowing the result of $a \wedge b$, it is not possible to determine the inputs of a, b. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low-power CMOS design, optical computing, nanotechnology and quantum computing.

The most prominent application of reversible logic lies in quantum computers [1]. A quantum computer will be viewed as a quantum network composed of quantum logic gates, each gate performing an elementary unitary operation on one, two or more two-state quantum systems called qubits. Each qubit represents an elementary unit of information, corresponding to the classical bit values 0 and 1. Any unitary operation is reversible hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts. Thus, quantum arithmetic must be built from reversible logical components [4].

One of the main constraints in reversible logic is to minimize the number of reversible gates used and garbage output produced. Garbage output refers to the output that is not used for further computations. In other words, it is not used as a primary output or as an input to other gate. Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated by knowing the number of primitive reversible logic gates required to realize the circuit. There are many numbers of existing reversible gates such as Toffoli gate [5], Feynman gate [6], Peres gate [7] in the literature. Quantum cost of Toffoli gate is 5, Feynman gate is 1, and Peres gate is 4. In this paper, a new reversible 4×4 SMG gate has been proposed. The conventional circuit considered in this work is four bit two's complement adder/subtractor [8]. Three designs have been proposed to implement the reversible four bit adder/subtractor, first one based on the Toffoli and Feynman gates, second one based on the Peres gate and the third one based on the proposed SMG gate.

PROPOSED 4×4 REVERSIBLE GATE

The proposed reversible SMG gate is shown in figure 1. One of the prominent functionality of the proposed gate is that it can work singly as a reversible full adder unit. Figure 2 shows the implementation of the proposed gate as the full adder. Reversible full adders are constructed using Toffoli and Feynman gates, Peres gate and the proposed SMG gate. The quantum cost for the reversible full adder constructed using Toffoli and Feynman gate is 12, full adder constructed using Peres gate is 8 and full adder constructed using SMG gate is 6.

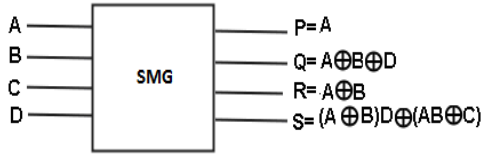


Figure 1: SMG gate

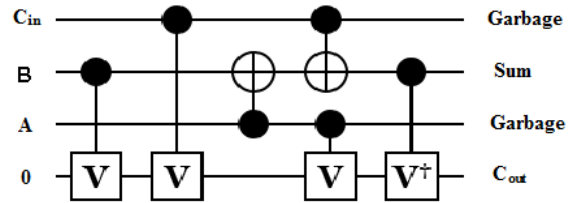


Figure 2: Proposed SMG gate as Full Adder

FOUR-BIT TWO's COMPLEMENT ADDER/SUBTRACTOR

The conventional circuit considered in this work is four bit two's complement adder/subtractor is shown in figure 3. When S is low, the B bits pass through the controlled inverter to the full adders. Therefore the full adders produce the sum of A and B. When S is high, the B bits are inverted before reaching the full adders. Also, a high S adds a 1 to the first full adder. This addition of 1 forms the 2's complement of B. Therefore the output of the full adders is the difference of A and B.

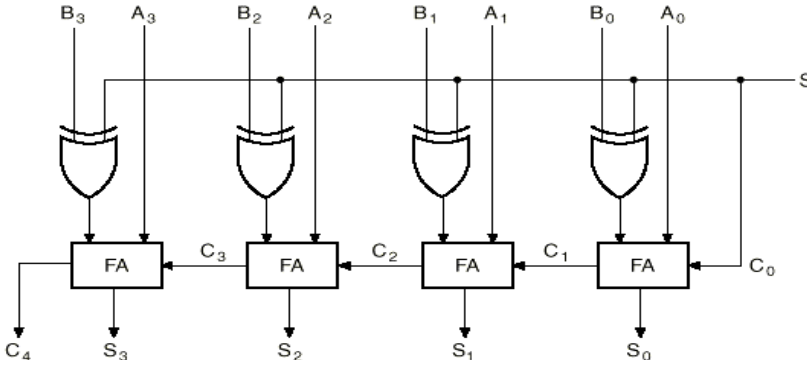


Figure 3: Four-bit Two's complement adder/subtractor

In this paper, three design types, DESIGN I, DESIGN II and DESIGN III of reversible four-bit two's complement adder/subtractor are proposed. DESIGN I is constructed using Toffoli and Feynman gates, DESIGN II is constructed using Peres gate and DESIGN III is constructed using SMG gate. The comparison of the designs in terms of number of reversible gates used, number of constant inputs, number of garbage outputs and quantum cost is shown in Table 1.

Table 1: Comparison of Reversible four bit two's complement adder/subtractor

	Number of Constant inputs	Number of Garbage outputs	Number of Reversible gates	Quantum cost
DESIGN I	4	1	20	52
DESIGN II	4	1	12	36
DESIGN III	4	1	8	28

According to the obtained result, DESIGN III using SMG gate is more optimal than the other designs. The proposed circuits have been simulated using QCviewer[9] and obtained results of simulation shows the correct operation of circuits. The proposed 4-bit two's complement adder/subtractor can be generalized for reversible n-bit two's complement adder/subtractor. The proposed circuits can be used to design large reversible systems. In a nutshell, the advent of reversible logic will significantly contribute in reducing the power consumption. Thus, the paper provides the initial threshold to build more complex systems which can execute more complicated operations.

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