A New Reversible SMG Gate and its application for designing Reversible Two's Complement Adder/Subtractor

Manjula Gandhi S[1] * Devishree J[2] † Sathish Mohan S[3] ‡

[1] *Assistant Professor (SG), Dept. of MCA, Coimbatore Institute of Technology, Coimbatore, Tamil Nadu, India*
[2] *Assistant Professor (SG), Dept. of EEE, Coimbatore Institute of Technology, Coimbatore, Tamil Nadu, India*
[3] *Senior Manager, Enterprise Information Management, Cognizant Technology Solutions, Coimbatore, Tamil Nadu, India*

Abstract. Reversible computation plays an important role in the synthesis of circuits which have application in quantum computing, low power CMOS design, bioinformatics and nanotechnology based systems. Conventional logical circuits are not reversible. A reversible circuit maps each input vector, into a unique output vector and vice versa. A new $4 * 4$ reversible full adder gate called as SMG gate is suggested in this paper. Three approaches to design reversible two's complement adder/subtractor are also proposed for the first time in the literature. The first approach is based on the Toffoli and Feynman gates, second approach is based on the Peres gate and the third approach is based on the new SMG gate. The proposed reversible adder/subtractor circuits are evaluated in terms of quantum cost.

Keywords: Reversible gates, Quantum Computer, Quantum cost, Quantum gates, two's complement adder/subtractor

1 INTRODUCTION

Many scientists say that single atom transistor is the end of Moore's Law", which states that within a period of 18 months the number of transistors in an IC doubles all along with its efficiency. He also predicted that the addition of extra number of transistors will not be possible in next few years and even if so, it may cause power consumption problems. Also, according to Landauer's principle, loss of 1 bit of information dissipates at least $kTln_2$ joule of energy, where $k = 1.3806505 * 10^{-23} m^2 kgs^{-2} k^{-1}$ (Joule/Kelvin) is the Boltzman constant and T is the operating temperature [4]. Bennett showed that $kTln_2$ energy dissipation would not occur if a computation is carried out in a reversible way [2]. The design that does not result in information loss is reversible.The most prominent application of reversible logic [5] lies in quantum computers [6].

2 PROPOSED REVERSIBLE GATE

The proposed reversible SMG gate is shown in Figure 1. One of the prominent function of the proposed gate is that it can work as a single reversible full adder unit. The inputs Cin, B, A are given in qubit1, qubit2 and qubit3 respectively. The outputs Sum and Cout are measured in qubit2 and qubit4 respectively. Hence, when the input is $|0110>$, the output is $|0011>$. Reversible full adders are constructed using Toffoli and Feynman gates, Peres gate and the proposed SMG gate. The quantum cost for the reversible full adder constructed using Toffoli and Feynman gate is 12, full adder constructed using Peres gate is 8 and full adder constructed using SMG gate is 6.

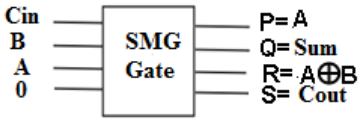

Figure 1: SMG gate

3 FOUR-BIT TWO's COMPLEMENT ADDER/SUBTRACTOR

The conventional circuit considered in this work is four bit two's complement adder/subtractor [3] is shown in Figure 2. When S is low, the B bits pass through the controlled inverter to the full adders. Therefore the full adders produce the sum of A and B. When S is high, the B bits are inverted before reaching the full adders. Also, a high S adds a 1 to the first full adder. This addition of 1 forms the 2's complement of B. Therefore the output of the full adders is the difference of A and B. In this paper, three design types, DESIGN I,

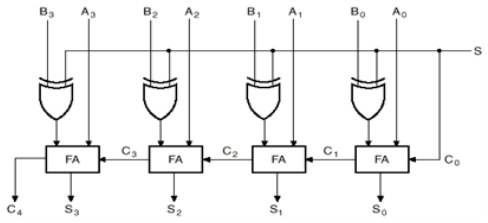

Figure 2: Four-bit Two's complement adder/subtractor

DESIGN II and DESIGN III of reversible four-bit two's complement adder/subtractor are proposed. DESIGN I

*manjulagandhi@cit.edu.in
†devishree@cit.edu.in
‡sathishmohan.selvaraj@cognizant.com

is constructed using Toffoli and Feynman gates, DESIGN II is constructed using Peres gate and DESIGN III is constructed using SMG gate.

3.1 DESIGN I

Design I of reversible two's complement adder/subtractor is constructed using Toffoli and Feynman gates. To add/subtract two four bit binary numbers the input is $|A_0B_0SS0A_1B_1S0A_2B_2S0A_3B_3S0 >$ and the outputs S_0, S_1, S_2, S_3 are measured in qubit4, qubit8, qubit12, qubit16 respectively. The reversible circuit of this design is given in Figure 3.

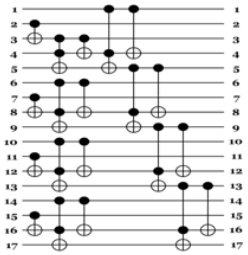

Figure 3: Reversible 2's complement adder/subtractor Design I

3.2 DESIGN II

In design II, Peres gates have been used. To add/subtract two four bit binary number the input is $|A_0B_0SS0A_1B_1S0A_2B_2S0A_3B_3S0 >$ and the outputs S_0, S_1, S_2, S_3 are measured in qubit4, qubit5, qubit9, qubit13 respectively. The reversible circuit of this design is given in Figure 4.

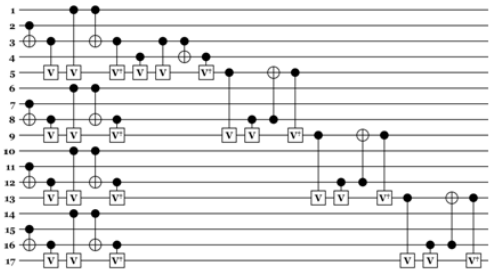

Figure 4: Reversible 2's complement adder/subtractor Design II

3.3 DESIGN III

In design III, SMG gate have been used. To add/subtract two four bit binary number the input is $|SB_0SA_00B_1SA_10B_2SA_20B_3SA_30 >$ and the outputs S_0, S_1, S_2, S_3 are measured in qubit3, qubit7, qubit11, qubit15 respectively. The reversible circuit of this design is given in Figure 5. To add 9(1001) and 3(0011), the value of S is 0, hence the input is $|01010100000000010 >$, the output is 01011100101000110, measuring the required qubits qubit15 is 1, qubit11 is 1, qubit7 is 0 and qubit3 is 0, hence the output is 1100(12).

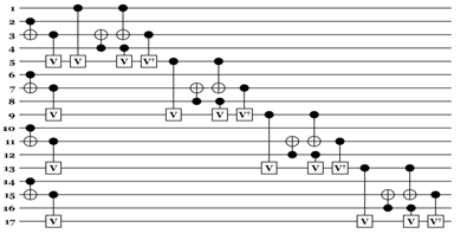

Figure 5: Reversible 2's complement adder/subtractor Design III

4 RESULTS

The comparison of the designs in terms of quantum cost is shown in Table 1.

Table 1: Comparison of Quantum Cost

Circuits	Quantum Cost
DESIGN I	52
DESIGN II	36
DESIGN III	28

According to the obtained result, DESIGN III using SMG gate is more optimal than the other designs. The proposed circuits have been simulated using QCviewer[1] and obtained results of simulation shows the correct operation of circuits. The proposed 4-bit two's complement adder/subtractor can be generalized for reversible n-bit two's complement adder/subtractor.

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